Design, Fabrication, Assembly and Characterization of a SWNT Switch for Non-volatile Memory Applications

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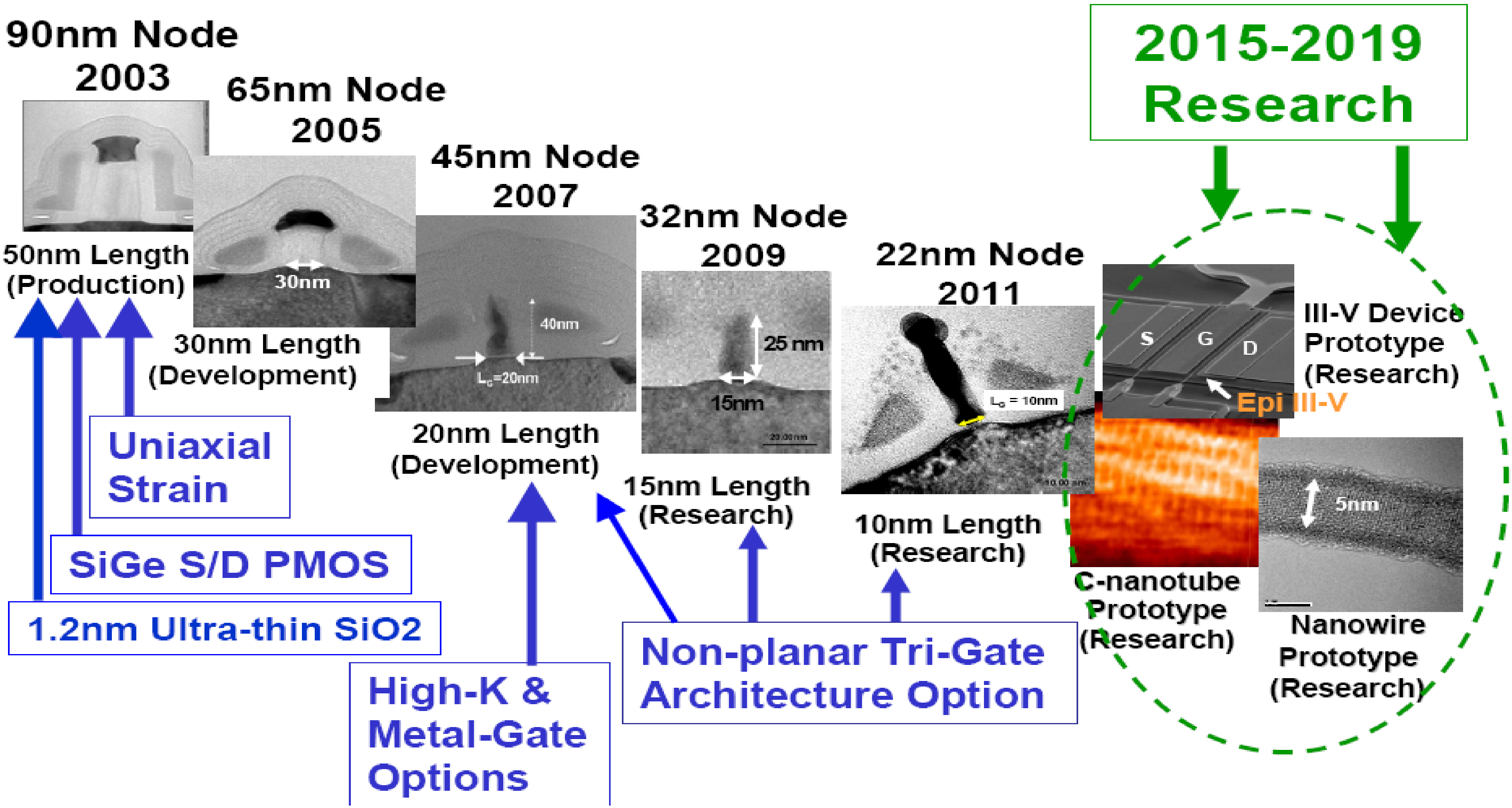
Outline

- State of Art
- Bi-stable Switch-Principle of Operation
- Fabrication
- Directed Assembly
- Actuation
- Product Attributes
- Summary

Beyond the ITRS Road map?

Transistor Scaling and Research Roadmap



CMOS Scale Limits and Power Considerations

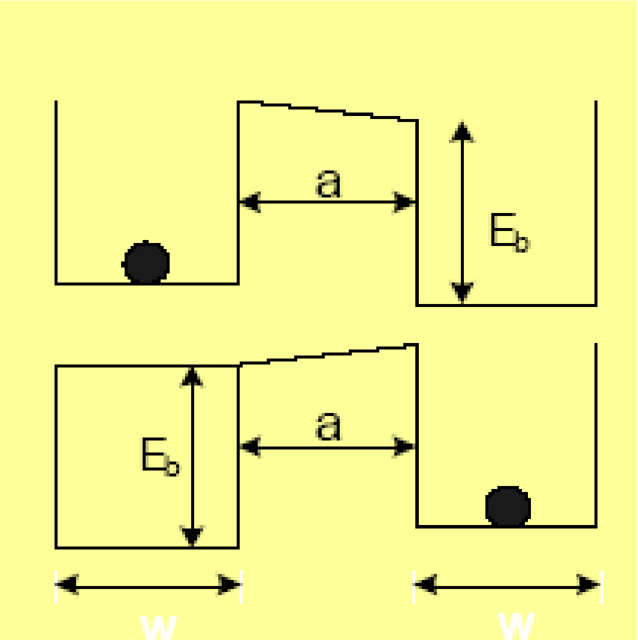
CMOS is projected to be with us for the next 15 years.

Theoretical[1] parameters at $T=T_{room}$

characteristic dimension of 1.5 nm,

switching energy of 0.017 eV

switching speed of 0.04 pico sec.



Theoretical[1] results:

1% duty cycle &

1% active transistors

Heat generated is ~ 370W/cm^2

1. Zhirnov, V., et. al., Proceedings IEEE, Nov. 2003

Nanoelectronics Challenges Examples of Non-Charge Based Switches

Novel Devices

What are we looking for?

- Required characteristics:
  - Scalability
  - Performance
  - Energy efficiency
  - Gain
  - Operational reliability
  - Room temp. operation
- Preferred approach:
  - CMOS process compatibility
  - CMOS architectural compatibility

Alternative state variables

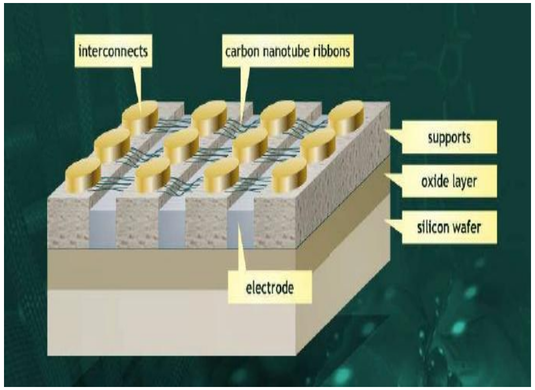
- **Spin–electron, nuclear, photon**
- **Phase**
- **Quantum state**
- **Magnetic flux quanta**
- **Mechanical deformation**
- **Dipole orientation**
- **Molecular state**

intel

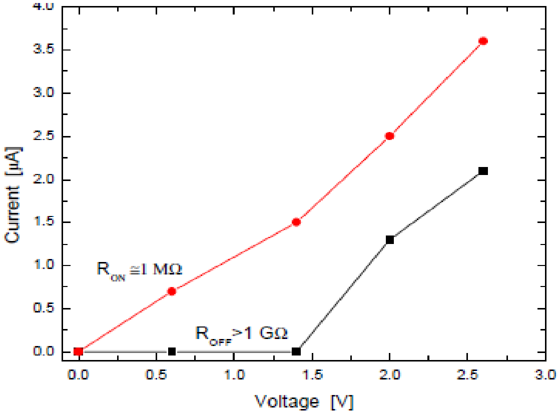
Intel Developer Forum

NEMS-Non volatile Design

NRAM

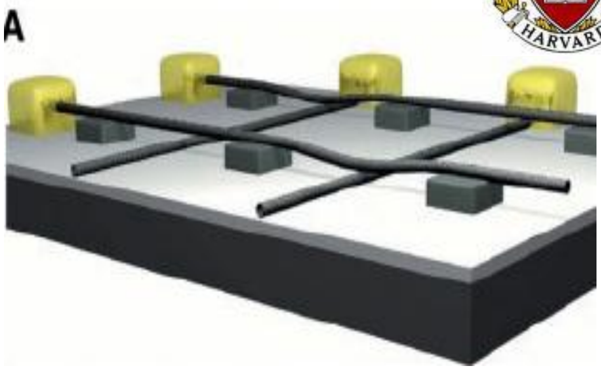


- Product (2004)
- SWNT Fabric
- Spin coated (Room Temperature)



$V_{Read} < 1.5$ V; $R_{ON}/R_{OFF} \sim 10^5$

Double Nanotube



- Concept (2000)
- Two single SWNT

Expected
$V_{Read} < 100$ mV;
$R_{ON}/R_{OFF} \sim 10^5$

NEMS → Memory & Embedded Applications.

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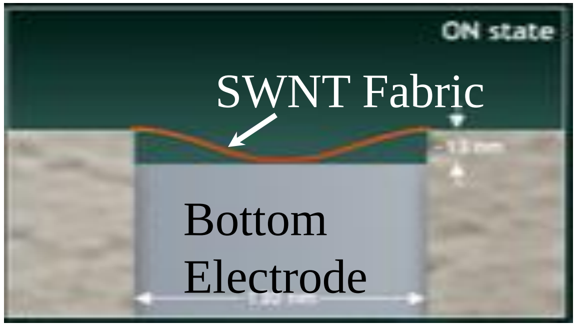
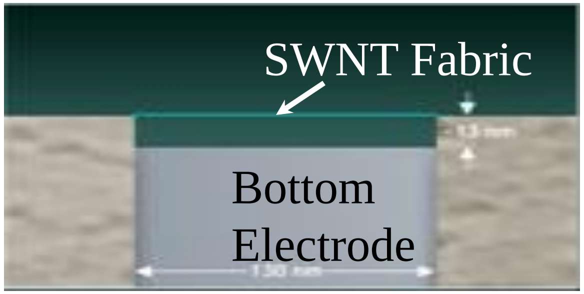
NEMS-Principle of operation

NRAM

WRITE
V_{write}=7V,
Closed Circuit ➔ R_{Low}
van der Waals attraction,



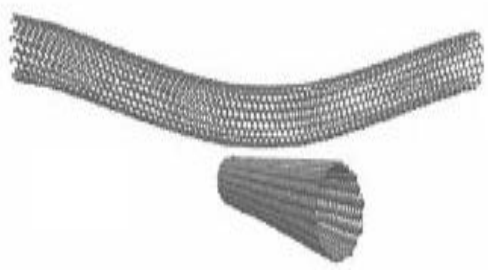
ERASE:
V_{Erase}=30V
Open Circuit ➔ R_{High}



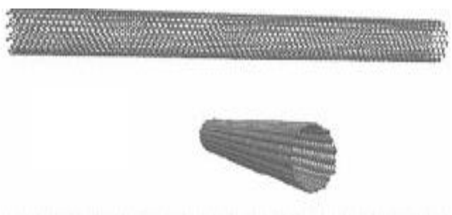
•**Memory Element**

DOUBLE NANOTUBE

WRITE
V_{write}=4.5V,
Closed Circuit ➔ R_{Low}
van der Waals attraction,



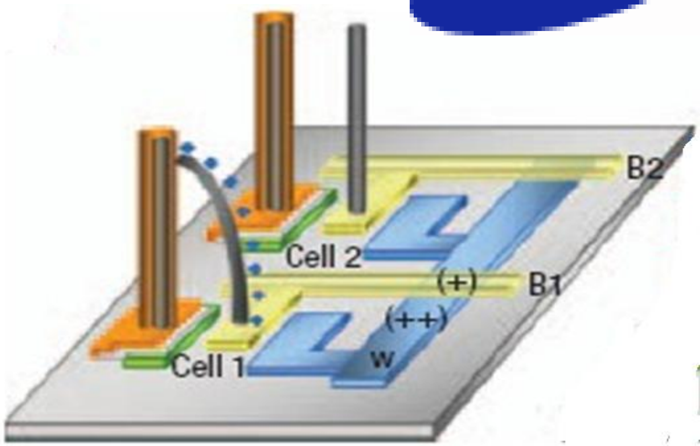
ERASE:
V_{Erase}=20V
Open Circuit ➔ R_{High}



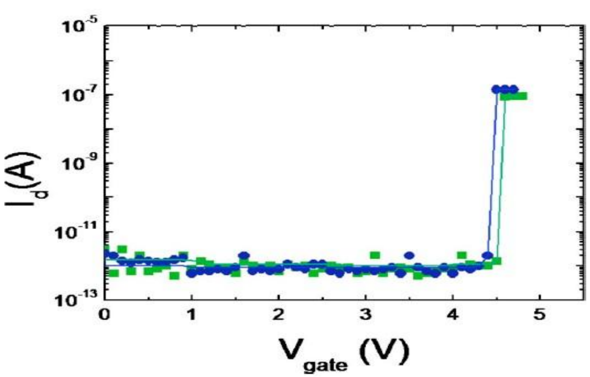
•**Memory Element**

NEMS-Volatile Design

Vertical Nanotubes SAMSUNG

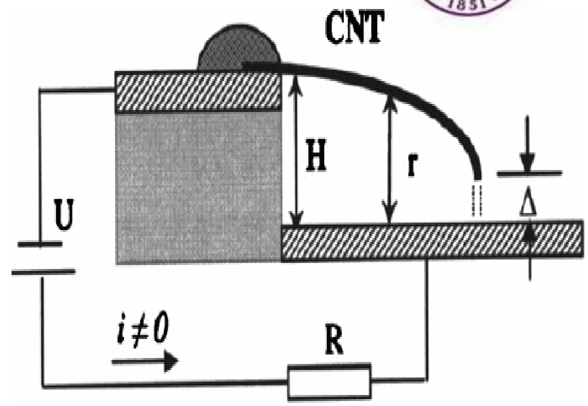


- Research Prototype 2005
- Capacitive based
- MWNT Pillars
- CVD grown (High Temperature)

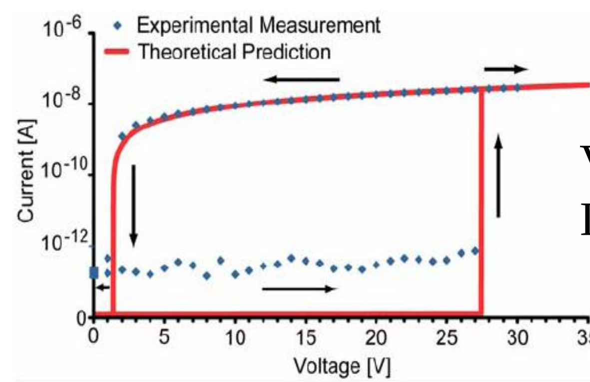


V_{switch} ~4.5V
I_{ON}/I_{OFF}~10^5

Cantilever



- Research Prototype 2004
- Resistive based
- MWNT
- Spin coated & CVD growth



V_{switch} ~22.5V
I_{ON}/I_{OFF}~10^4

NEMS ➔Embedded Applications.➔ Expected to replace DRAM

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NEMS-Principle of operation

Vertical Nanoswitch :

Write:

Apply 0.1V to Drain; Apply gate voltage to the 4.5V

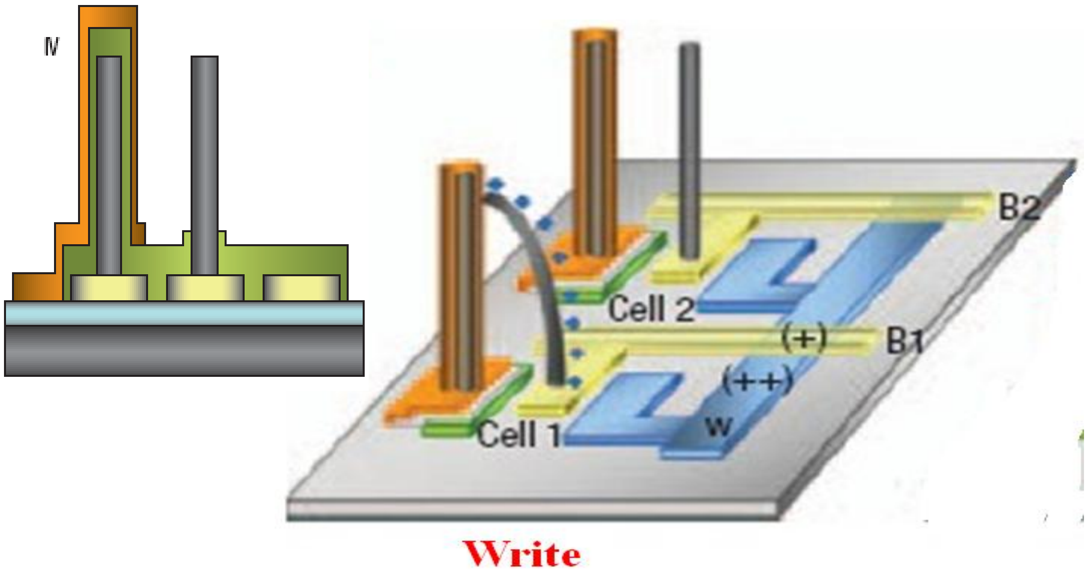
→CNT of Drain begins to bend and contacts the source

→Capacitor gets charged

Erase:

Removal of gate voltage→ Repulsive electrostatic force

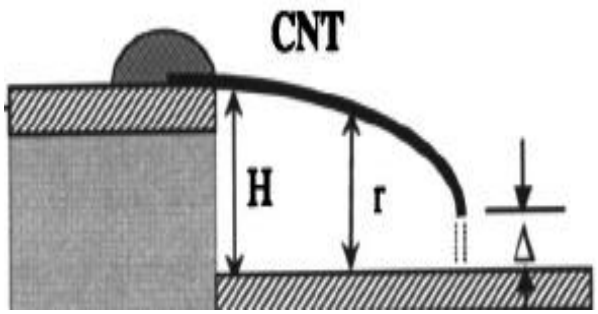
Drain nanotube springs back. → Capacitor Discharges



NEMS Cantilever

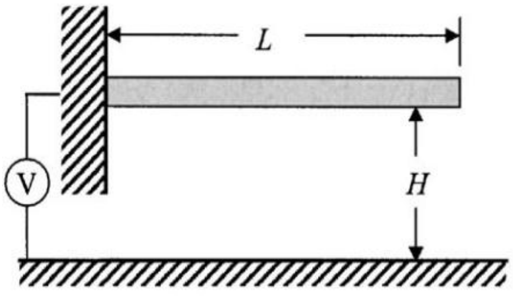
Write:

22V, tunneling current, 0.7nm gap



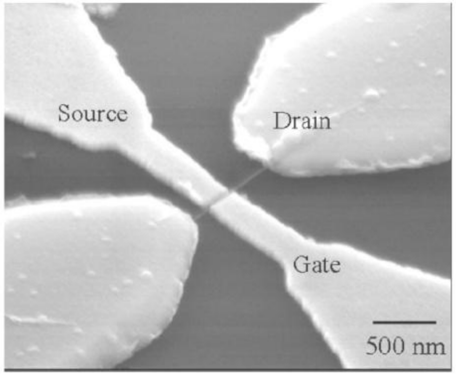
Erase

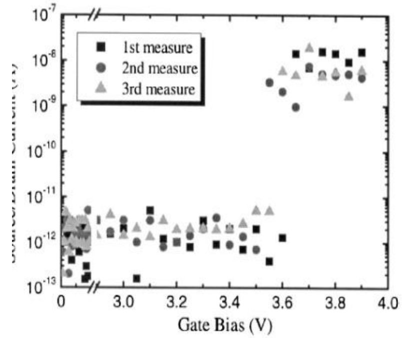
<2V, open circuit 100nm gap



NEMS – State of the Art

Large ~30nm MWNT

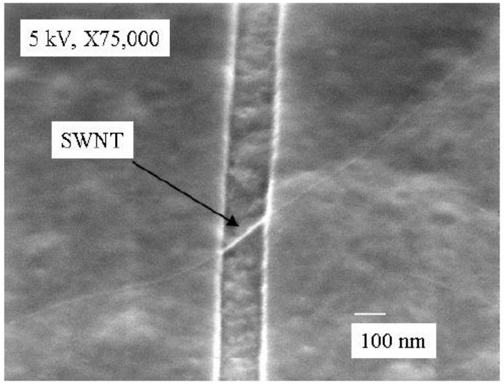


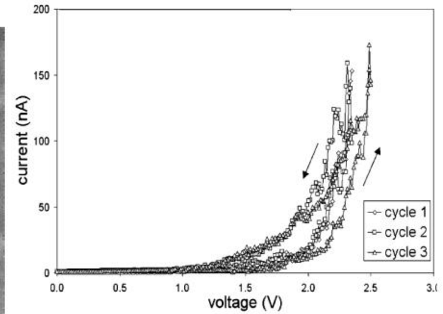


Only 3 Sweeps!

S. N. Cha, J. E. Jang, Y. Choi, G. A. J. Amaratunga, D. J. Kang, D. G. Hasko, J. E. Jung, and J. M. Kim, "Fabrication of a nanoelectromechanical switch using a suspended carbon nanotube," *Applied Physics Letters, vol. 86, p. 083105, 2005.*

Serial Process SWNT

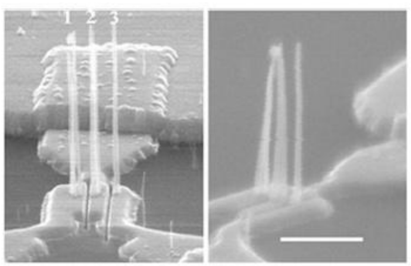




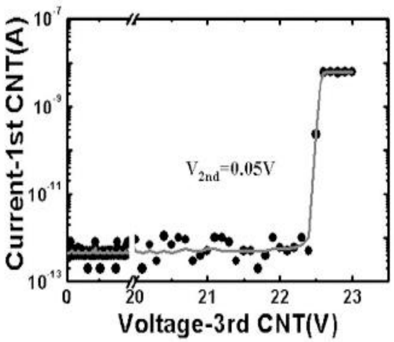
Only 3 Sweeps!

A. B. Kaul, E. W. Wong, L. Epp, and B. D. Hunt, "Electromechanical carbon nanotube switches for high-frequency applications," *Nano Lett, vol. 6, pp. 942-947, 2006.*

Huge 70nm MWNTs

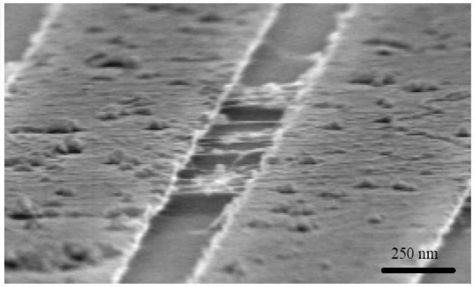


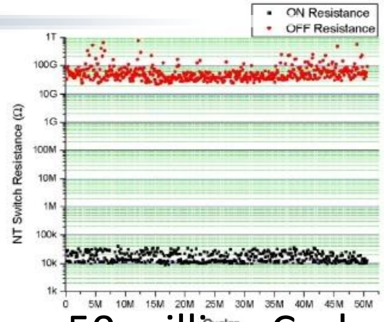
1 micron



J. Jang, S. Cha, Y. Choi, G. Amaratunga, D. Kang, D. Hasko, J. Jung, and J. Kim, "Nanoelectromechanical switches with vertically aligned carbon nanotubes," *Applied Physics Letters, vol. 87, p. 163114, 2005.*

Matt of SWNTs





50 million Cycles!

~10ns Response Time

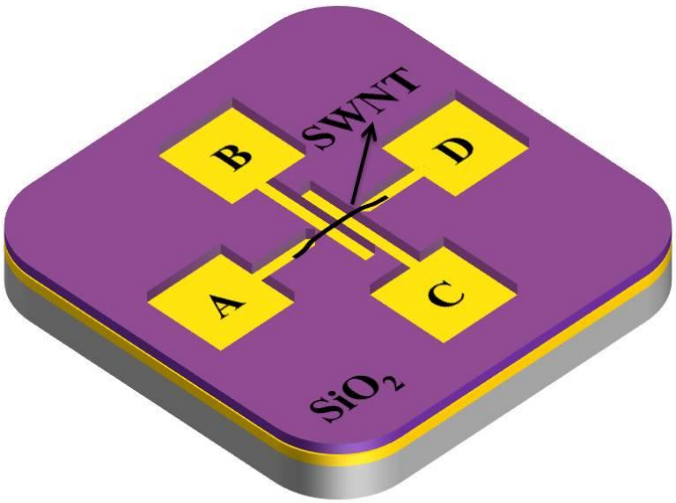
R. F. Smith, T. Rueckes, S. Konsek, J. W. Ward, D. K. Brock, and B. M. Segal, "Carbon nanotube based memory development and testing," 2007, pp. 1-5.

NANTERO

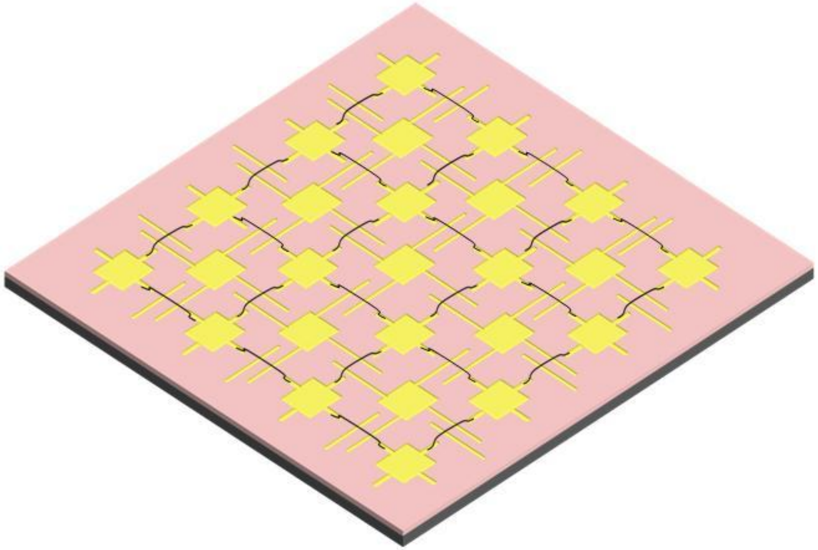
Bistable Nano Electromechanical Switch

Bistable SWNT Nanoswitch

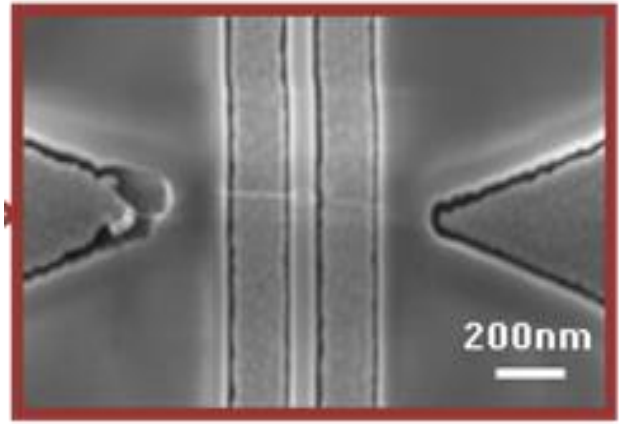
Schematic diagram



Switch array schematic



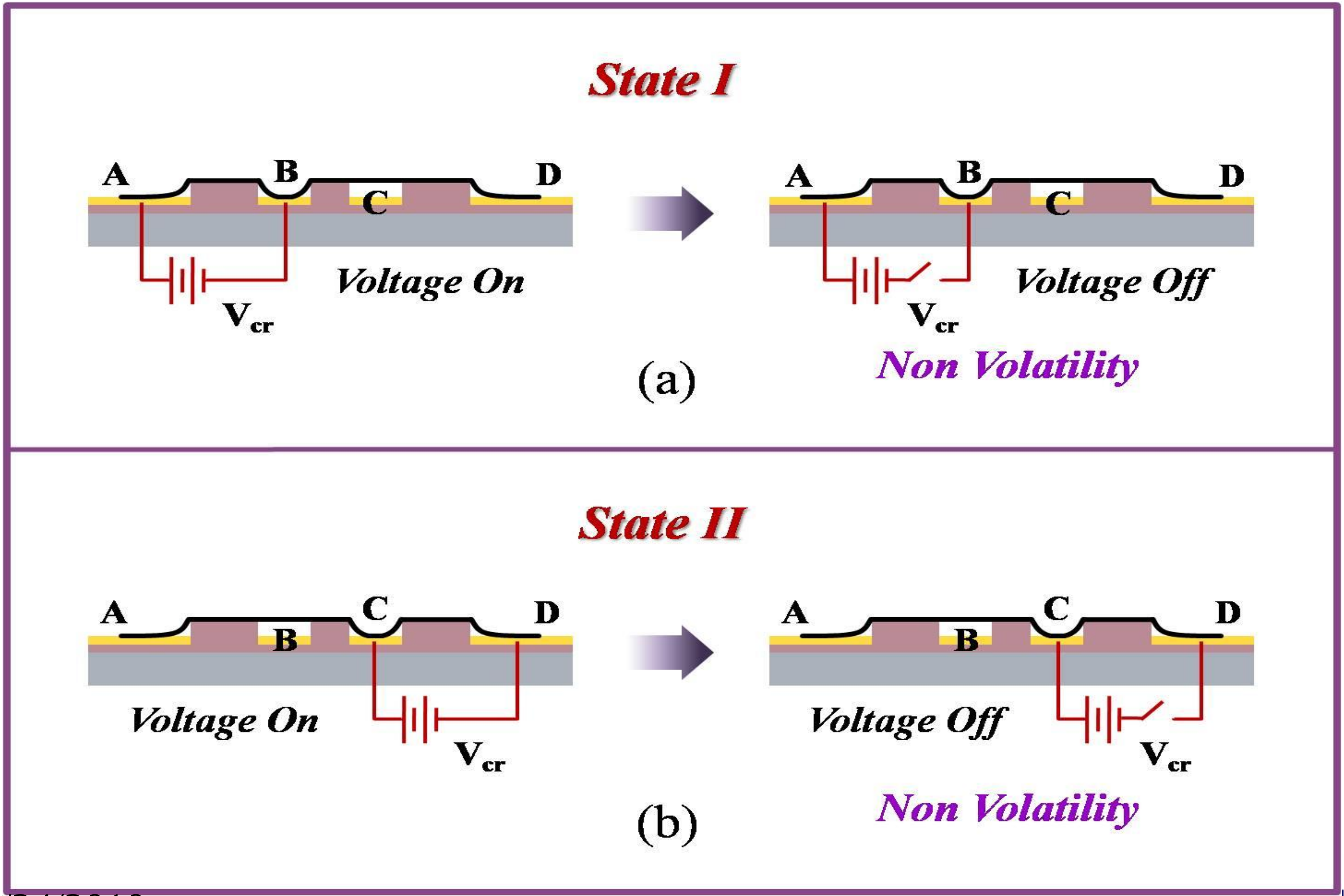
Top View of fabricated device



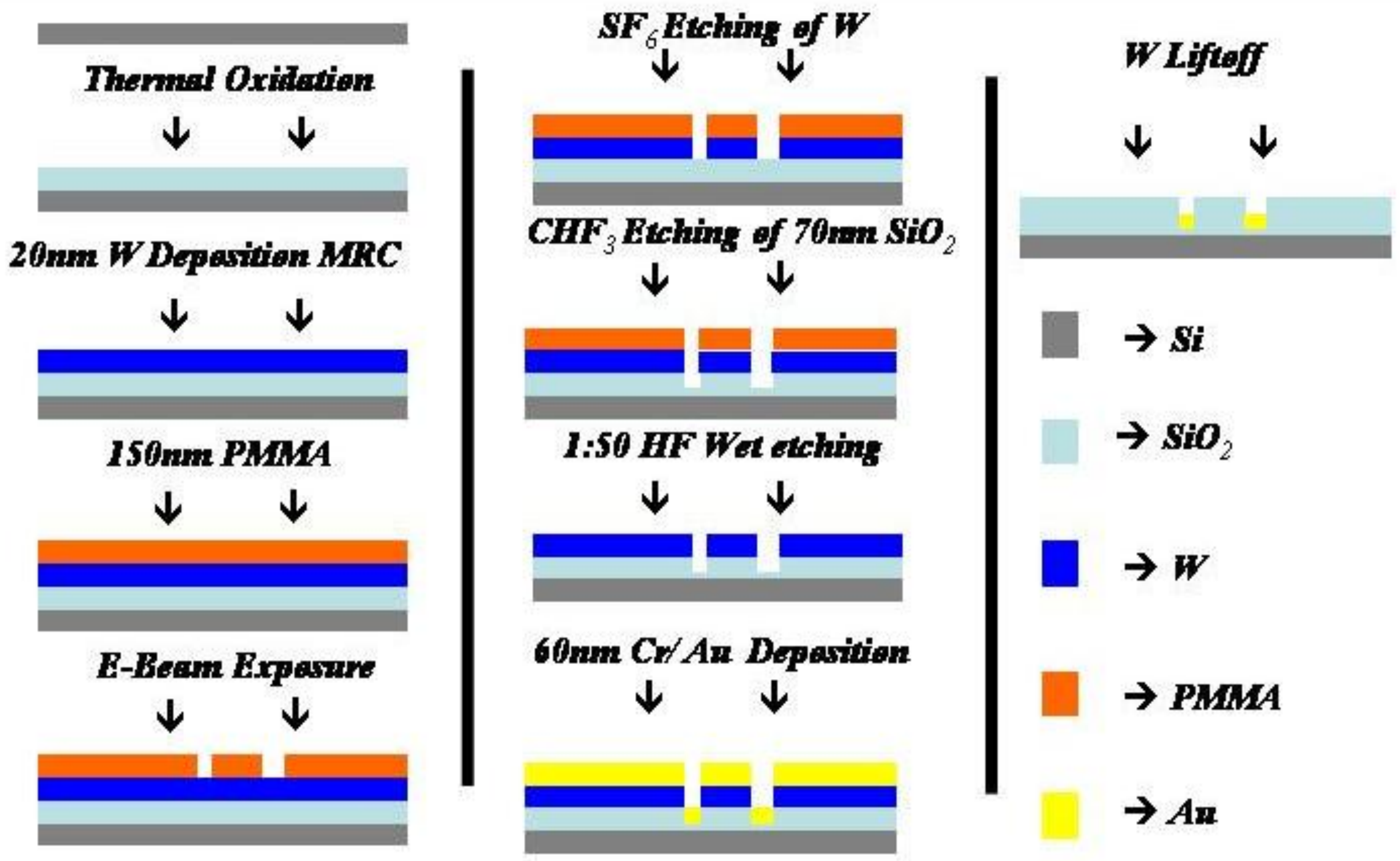
Advantages:

- Non charge based device
- Non volatile
- Minimal fabrication steps
- Operational frequency in terahertz
- Stand alone RS flip Flop
- Radiation hard
- Very robust.
- Switching at the same vc

Principle of Operation



Template Fabrication



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Directed assembly of SWNT

Dielectrophoretic Assembly of SWNTs

- **Dielectrophoretic force (F_{DEP})**

$$F_{DEP} = \frac{\pi}{6} r^2 l \varepsilon_m \mathrm{Re}\{K(\omega)\} \nabla E_{rms}^2$$

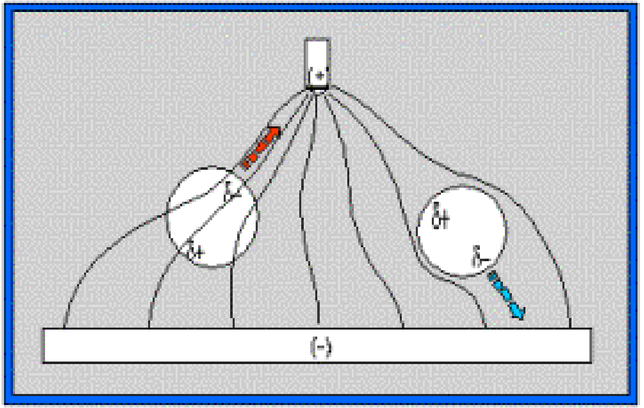
$$K(\omega) = \left(\frac{\varepsilon_p^* - \varepsilon_m^*}{\varepsilon_m^*} \right)$$

l: Length of rod-like particle, r: Radius of rod-like particle

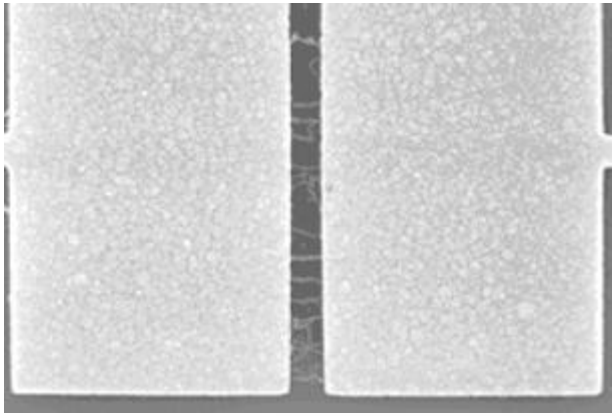
ε_m: Real permittivity of suspending medium

E_{rms}: Root mean square (rms) of the electric field

K(ω): Clausius-Mosotti factor

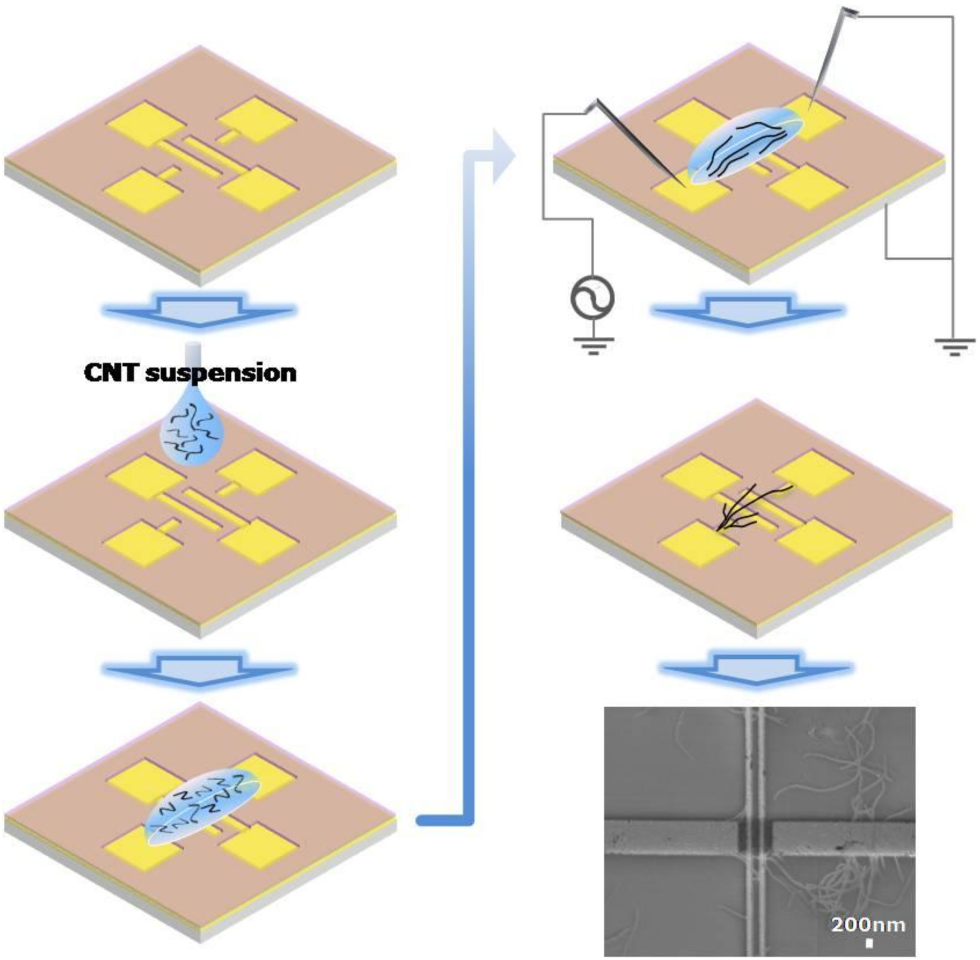


- **DEP force strongly depends on the electric field gradient, ΔE_{rms} .**



Dielectrophoretic Assembly of SWNTs

❖ **Conventional Dielectrophoretic Assembly Process of CNT**



- ✓ **Changed the electrode configuration.**
- ✓ **Introduced a phase shifter at the ground electrode with the potential being opposite in phase with that of the phase electrode.**
- ✓ **Drying a drop of CNT solution by employing stream line of N_2.**

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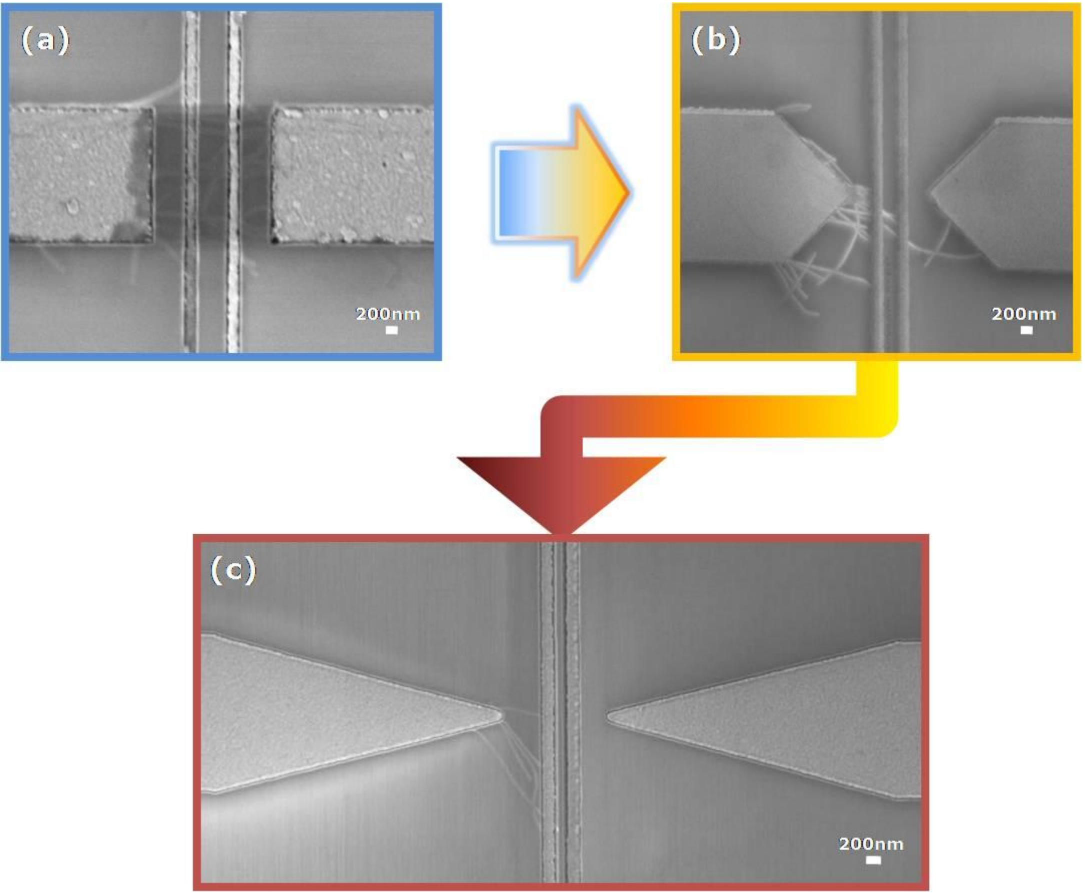
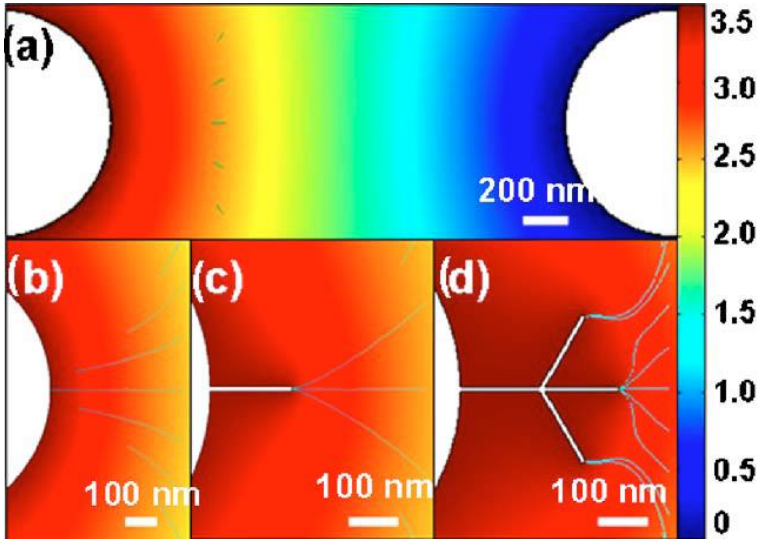
Dielectrophoretic Assembly of SWNTs

❖ **Modifications of Assembly Process of CNT**





Simulation

Changes of the electrode configuration:
(a) initial
(b) transition
(c) final

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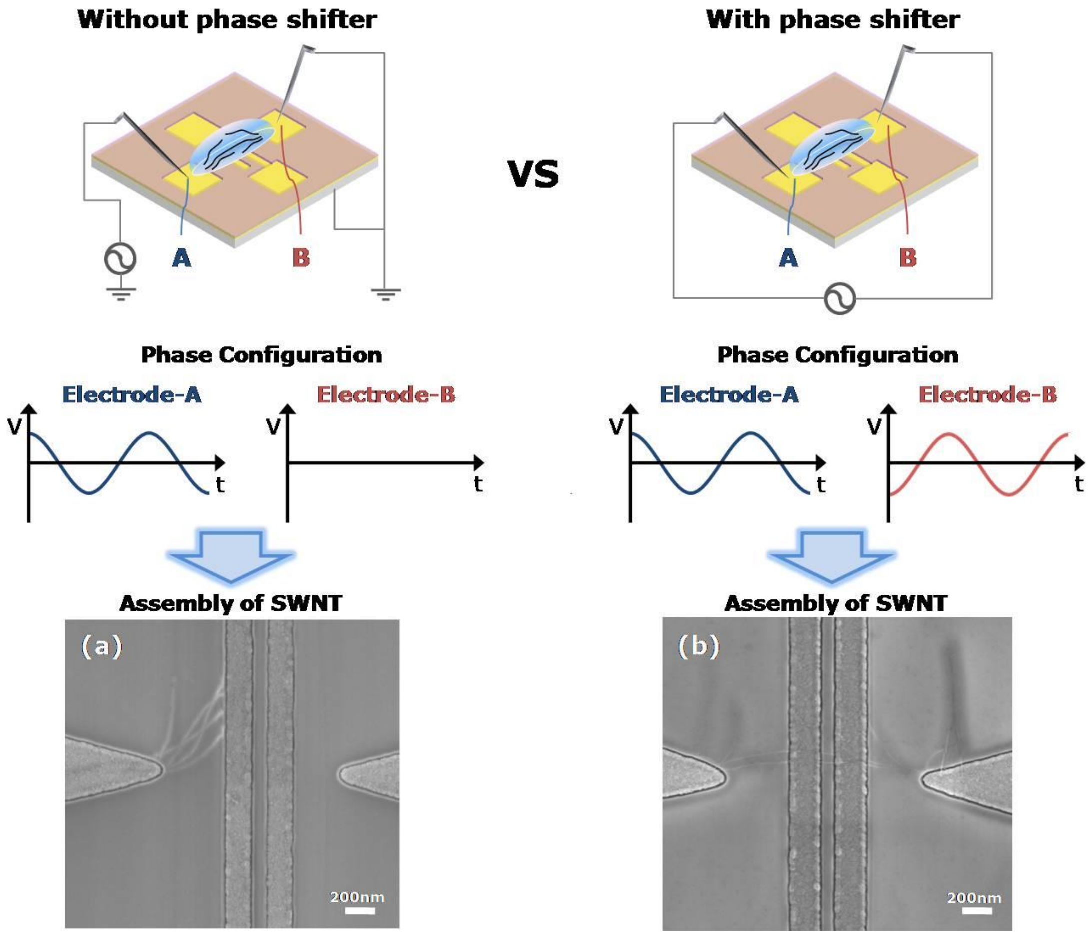
Dielectrophoretic Assembly of SWNTs

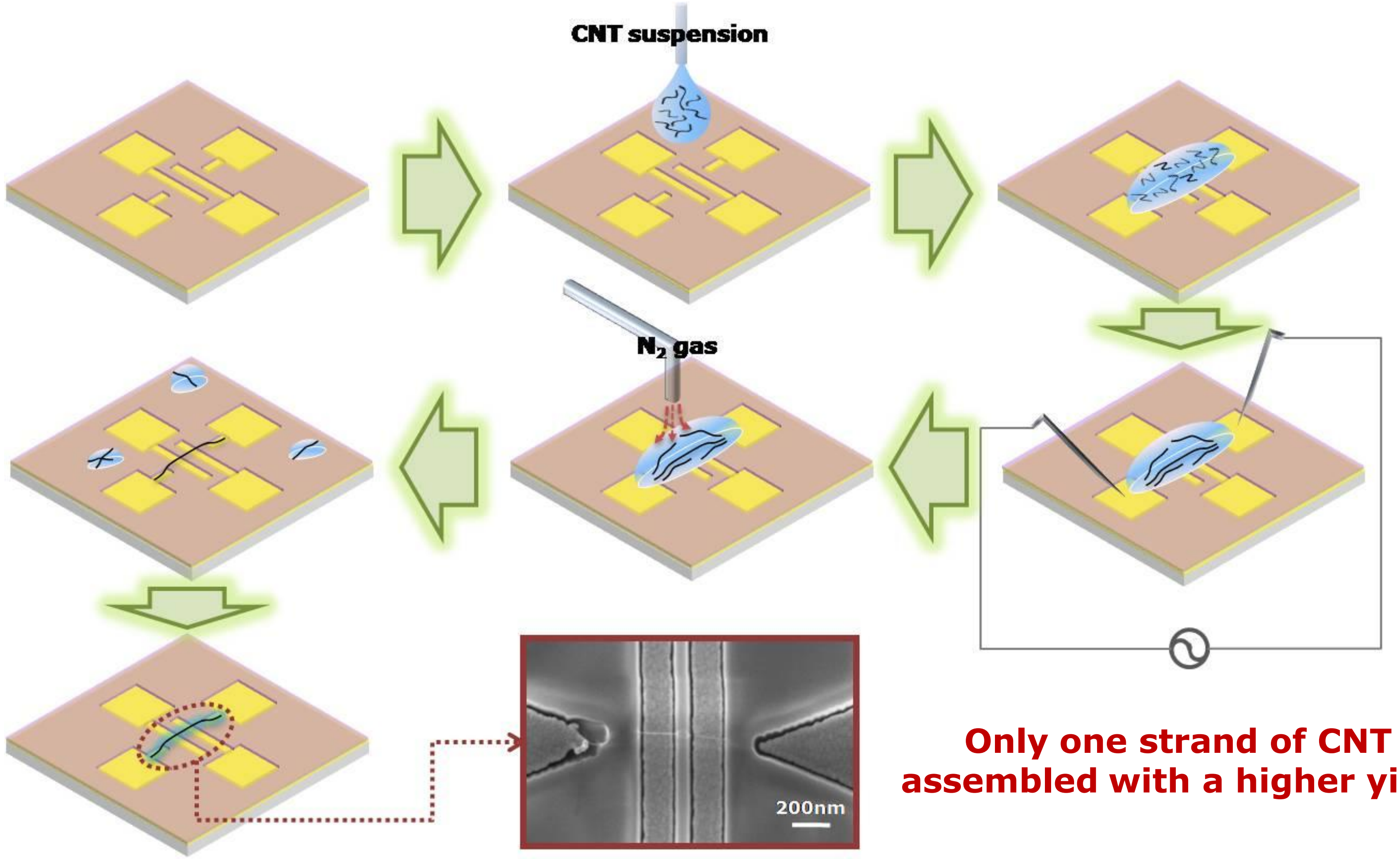
❖ **Modifications of Assembly Process of CNT**



Results of introducing a phase shifter at the ground electrode (electrode-B) being opposite in phase with that of the phase electrode (electrode-A)

Dielectrophoretic Assembly of SWNTs

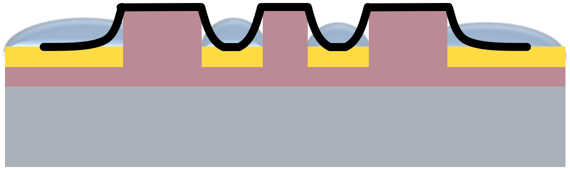
❖ **Modified Dielectrophoretic Assebmly Process of CNT**



Only one strand of CNT assembled with a higher yield

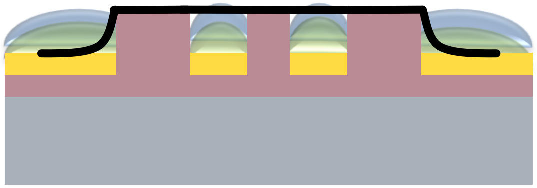
Dielectrophoretic Assembly of SWNTs

Problem: For a shallow trench during drying process the surface tension of the liquid (water) pulls in the SWNT into the trench causing short circiuted.

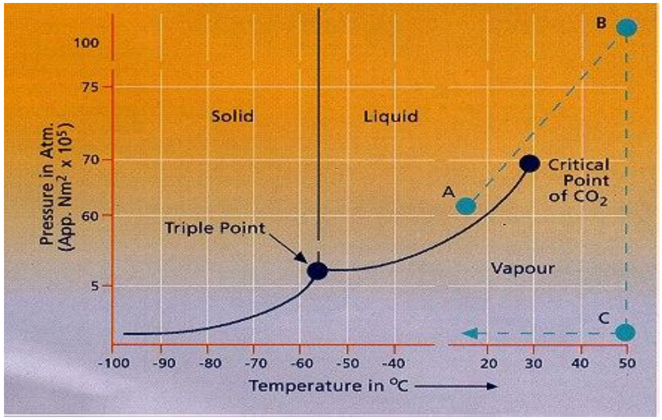


Solution:

Use a Critical point Dryer (CPD).



- **Critical Point Dryer**
  - ✓ **To make CNTs suspended above trenches**
  - ✓ **Dry process at critical point in CO_2 phase diagram**
  - ✓ **No phase transition**



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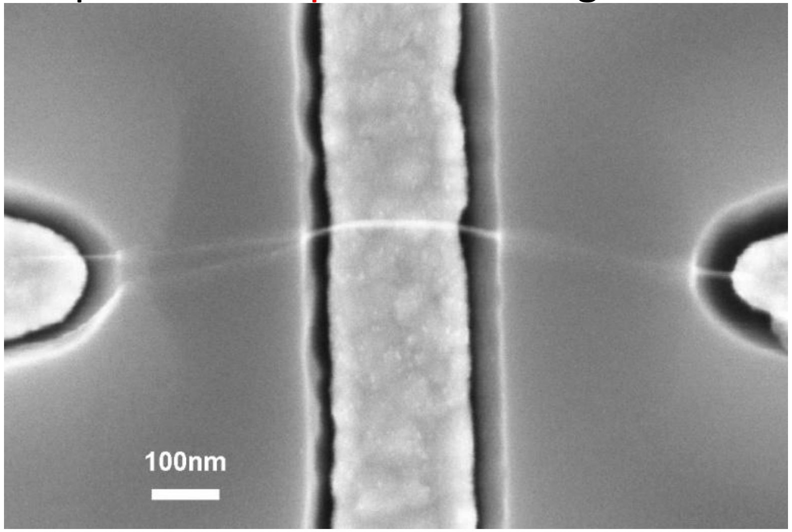
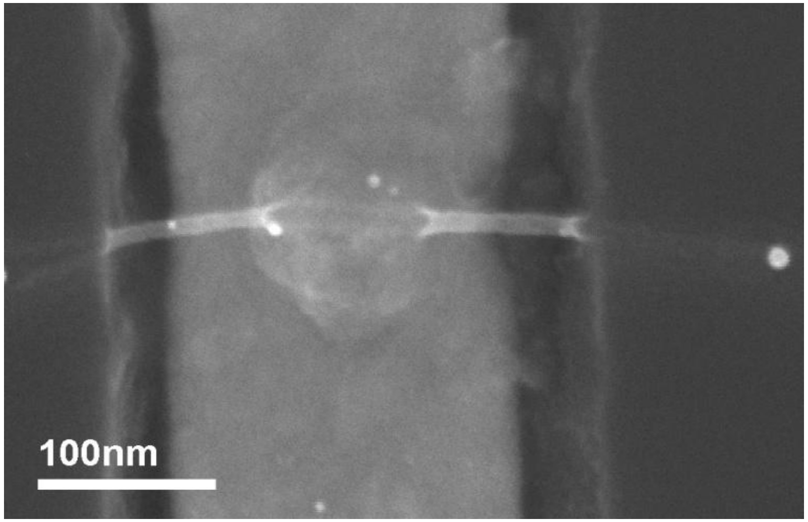
Actuation Preliminary Results

Actuation in Ambient Conditions

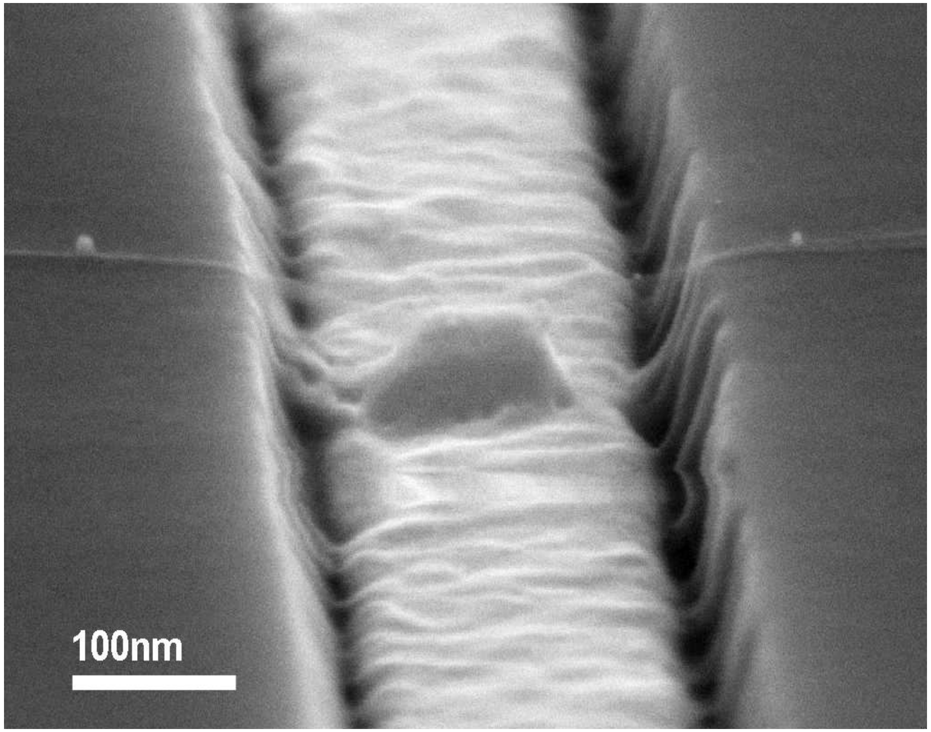
Top view SEM prior to testing in lab air





Top view SEM after testing in lab air

80 Degree SEM after testing in lab air



→ Organic contamination build up
→ Device needed to be tested in Nitrogen enviro

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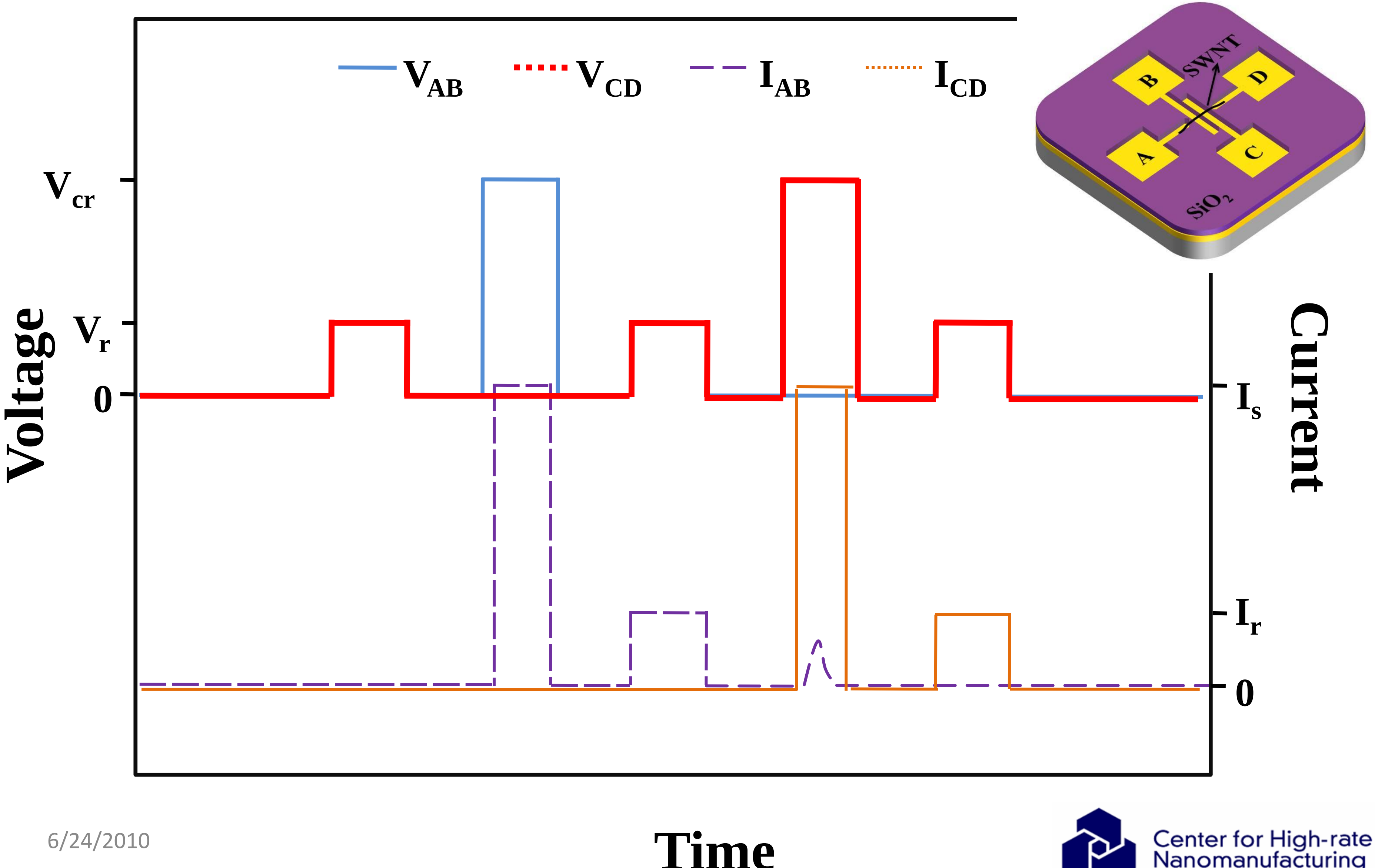
Actuation Schematic



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Product Attributes

Product Attributes

Bit density: Current Status (Concept; Prototype; Production)

	NRAM	Bistable Nanoswitch	Cantilever	Vertical Nanoswitch	Double Nanotube*	NAND Flash
Feature Size	180nm	180nm	500nm	No Data	10nm	40nm
Factor	$6F^2$	$12F^2$	$6F^2$	No data	$6F^2$	$4F^2$
Cell Size	$0.19\mu m^2$	$0.38\mu m^2$	$1.5\mu m^2$	No data	$0.0006\mu m^2$	$0.0064\mu m^2$
Storage density	$3.09Gb/in^2$	$1.55Gb/in^2$	$0.6Gb/in^2$	$2.5Gb/in^2$	$1000Gb/in^2$	$62.9Gb/in^2$

➔Cell factor remains same with scaling down   * ➔ Has never been fabricated (estimated values)

Power Consumption

Energy/ Power	NRAM	Bi stable	Cantilever	Vertical Nanoswitch	Double Nanotube*	NAND Flash
Read	1.5fJ/ 0.15 µW	1.5fJ/ 0.15 µW	0.25fJ/ 0.025µW	1zJ-0.16fJ/ 1pW-0.1µW	1.5fJ/ 0.15 µW	0.165nJ/ 3300 µW
Write	7fJ/ 0.7µW	4.5fJ/ 0.45µW	2.3fJ/ 0.23 µW	7.2fJ/ 4.5 µW	4.5fJ/ 0.45µm	1.87nJ/ 2 µW
Erase	30fJ/ 3 µW	4.5fJ/ 0.15 µW	2zJ/ 0.2pW	160zJ/ 1pW	20fJ/ 2 µW	0.33nJ/ 3.3 µW

➔ Power decreases non-linearly with scaling down   * ➔ Estimated values

Product Attributes

Read, Write, Erase Time

NAND write and erase is in Pages and Blocks

➔High speed, faster than flash and comparable to SRAM

➔ Speed increases non linearly with scaling down

➔ Non destructive read (No rewrite)

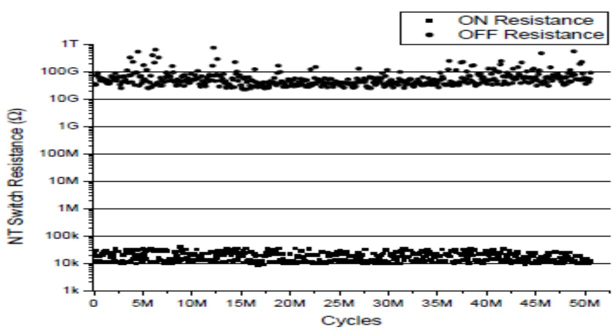
Speed	NRAM	Bistable	Cantilever	Vertical Nanoswitch	Double Nanotube*	NAND Flash
Read	10ns	10ns	1-10ns	1.3ns-16ns	0.01ns	30µs/4224bits
Write	10ns	10ns	1-10ns	1.3ns-16ns	0.01ns	200µs/4224bits
Erase	10ns	10ns	1-10ns	1.3ns-16ns	0.01ns	2ms/135168bits

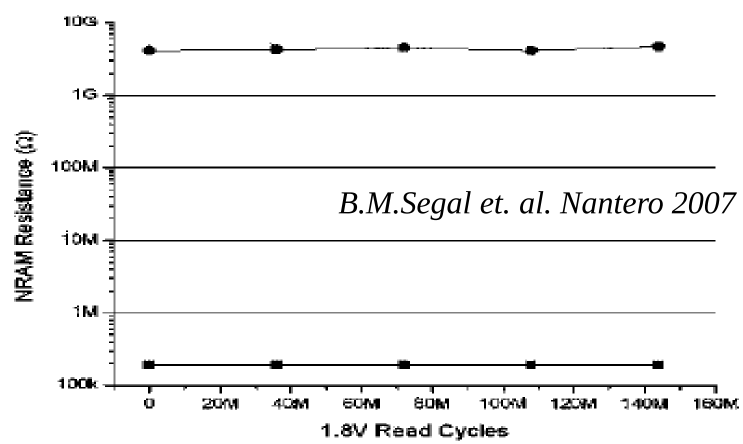
* ➔ Have never been fabricated (estimated values)

Endurance

• Devices have cycled ~ $5X10^7$ for Write/Erase and ~$1.5X10^8$ Read with no failure issues.

•Others devices are expected to have similar endurances.





Flash endurance is only 10^5 cycles

Summary

- Have fabricated a Bi-stable switch for memory and logic application
- Employed a modified Dielectrophoresis process for assembly of SWNTs
- Switch actuation showed that the switch is nonvolatile
- Switch actuation showed that the switch is indeed bi-stable
- Switch actuation is carried out at low voltage (~5V)